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U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
	AA						
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FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Abstract Yes	Abstract No
/PS/	AG	2002-279333	9/2002	JP			X	
/PS/	AH	2000-035898	2/2000	JP			X	
/PS/	AI	07-084832	03/1995	JP			X	
/PS/	AJ	2 317 245 A	3/1998	GB			X	
/PS/	AK	10-116302	6/1998	JP			X	
	AL							
	AM							
	AN							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

/PS/	AO	M. IENAGA, et al.," Seiyo Shori Hardware no Koi Gosei no Tame no Kosoku na Menseki/Jikan Saitekika Algorithm", DA Symposium 2000, Information Processing Society of Japan, 17 July, 2000 (17/07/00), Vol. 2000, No. 8, pages 27 to 32.
-/PS/	AP	A. NAKATA, et al., "Deriving Parameter Conditions for Periodic Timed Automata Satisfying Real-Time Temporal Logic Formulas", Proc. of IFIP TCP/WG6. 1 Int. Conf. on Formal Techniques for Networked and Distributed Systems (FORTE2001),Kluwer Academic Publishers, 2001.08, pages 151-166.
/PS/	AQ	K. WAKABAYASHI, et al., Densoyo LSI o Dosa Gosei de Kaihatsu, Kino Sekkei no Kikan ga 1/10 ni Tanshuku", Nikkei Electronics, Nikkei Business Publications, Inc., 12 February, 1996, No. 655, pages 147-169.
/PS/	AR	H. OKEWATARI, et al., "Multi Processor ni yoru Bunsan Shori o Ishiki Shita Senyo Processor Sekkei Shien System SYARDS no Kochiiku", Information Processing Society of Japan Kenkyu Hokoku, Information Processing Society of Japan, 20 January, 1995, Vol. 95, No. 6 (DA-73), pages 105 – 112.
/PS/	AS	S. KITAGUCHI, et al., "Jitsujikan Seiyaku o Yusuru Tan'itsu Bus System no JAVA ni yoru Model-ka oyobi Parametric Model Checking o Mochita Sekkei Shuho no Teian", Information Processing Society of Japan Kenkyu Hokoku, Information Processing Society of Japan, 28 Nov. 2002, Vol. 2002, No. 113 (SLDM-107), pages 19 to 24.
/PS/	AT	"TAXYS: A Tool For the Development and Verification of Real-Time Embedded Systems" by E. CLOSSE, et al.
/PS/	AU	"Design and Implementation of Priority Queuing Mechanism On FPGA Using Concurrent Periodic EFSMs And Parametric Model Checking" by T. KITANI, et al.
/PS/	AV	"A Flexible and High-Reliable HW/SW Co-Design Method for Real-Time Embedded System" by T. KITANI, et al., pgs. 1-10.
/PS/	AW	"HY-C LRM 1.2 Rev 1.1" Y Explorations, Inc., Nov. 7, 2004.
	AX	
	AY	

/Patrick Sandoval/ (09/28/2007)